Investigation of different digital implementation methods for the TIGER radar receiver

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Abstract
This paper compares different techniques for digital implementation of the receiver section of the TIGER radar. Three methods are compared: the normal Direct Conversion method, the IF under sampling method and the RF sampling method. Differences in performance, required resources and noise effects are presented. The number of significant bits required by each method is also considered. Some simulation results using SPW are provided.

Index Terms
Digital receivers, IF, RF, SuperDARN.

I. INTRODUCTION

The Tasmanian International Environment Radar (TIGER) is an over-the-horizon radar that locates ionospheric structures in the region between Tasmania and Antarctica by measuring their velocities. Compared to other similar (SuperDARN) radars, TIGER is uniquely sited to detect phenomena occurring in the region equatorward of the normal auroral oval. A current project exploits this advantage to study the physical process generating phenomena that are poorly understood, such as sub-auroral convection flows and the generation of the plasmapause after magnetic storms. [1]-[3]

In recent years, the use of digital receiver technology has lead to an increase performance and reduction in cost. These digital techniques will soon replace many analogue functions as devices such as analog to digital converters keep on improving their speed and resolution. Improvements in digital hardware, such as larger and faster Field Programmable Gate Array (FPGA), are also helping digital implementations of traditional analog functions.[4].We are researching the digital implementation of the current analog TIGER radar system using FPGA devices.

The proposed digital receiver will work from 8-20MHz at 100KHz bandwidth. Compared with the analog design, the digital version can provide better performance and more flexibility since the system can be reprogrammed. An FPGA implementation was chosen because of the low cost and the inbuilt reconfigurability of FPGA devices. The proposed digital receiver will have the same specifications as the current analog receiver, however new digital techniques should allow greater configurability so that the receiver can be optimized for different operational modes. Different methods in digital implementation have been investigated and compared.

II. DIRECTION CONVERSION

In the early phase of digital era, the direction conversion method was the most popular since the available hardware power was only powerful enough to provide the digitization and processing of signal at the base band. In this method, the signal is down converted to base band using analog mixers and filters and then digitized at base band [7]. The block diagram for the direct conversion method is shown in figure 1

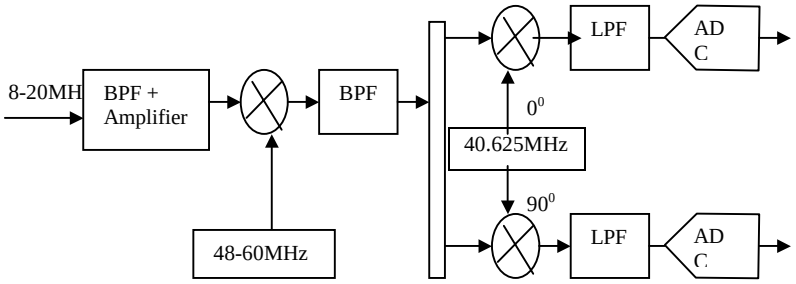

Figure 1. Block diagram of the base band digital techniques

Here, the modulated RF signal is up converted with the local oscillator to produce the IF signal at 40.625Mhz. Next, the signal is split and quadrature down converted to the base band using a local oscillator at 40.625 MHz. The base band product is selected with a low pass filter (LPF) to produce the I and Q components before digitization. This method uses less resource since the signal is converted to the digital domain at base band. It does not require fast ADC and processing resources. For the signal bandwidth of 100KHz, a 16-bit ADC operating at 300Khz can satisfy the requirements. Also a DSP processor (as well as an FPGA) can handle the signal at this sampling frequency. However, because most of the components are analog, this design has several disadvantages. The filters can introduce gain and phase imbalance, the mixer can also distort the signal and there can be a phase imbalance between the I and Q channels. The parameters of the components will also change with environment parameters such as temperature and humidity. These effects can cause loss of performance of the receiver, and the advantages over a fully analog implementation are limited, particularly for this radar application where there is no specific base band modulation to be detected.

III. IF UNDER SAMPLING WITH POLYPHASE FILTERING

The block diagram of the IF under sampling method is shown in figure 2

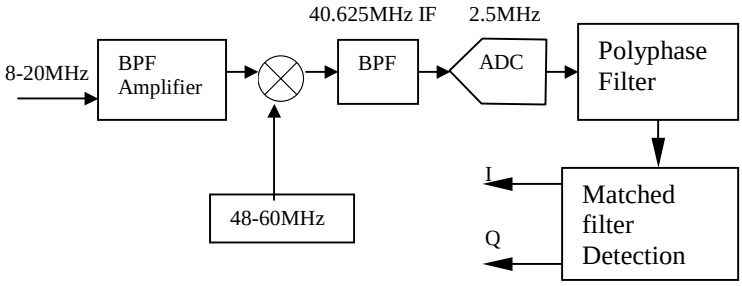

Figure 2. Block diagram of the IF under sampling with Polyphase filtering method

In this method, the ADC has been moved to the IF output. According to Nyquist theorem, the sampling rate must be at least twice the greatest frequency to prevent aliasing effects. In this design, the carrier frequency is 40.625 MHz; hence the minimum Nyquist requirement is 81.25 MHz. However, if the signal is sampled at frequency lower than the Nyquist rate, it can be intentionally aliased to the desired frequency. Thus performing a controllable frequency shift. The aliased frequency will be "fc mod fs" (where fc and fs are carrier frequency and sampling frequency respectively). [5]-[6].

$$f_{aliased} = fc(\text{mod})\, fs$$

If the signal is sampled at 2.5MHz with 16bits resolution this represents heavy over sampling compared to the bandwidth. Our signal is aliased to 0.625MHz (40.625MHz (mod) 2.5MHz). The noise in this 0.625MHz bandwidth (and other aliased frequencies) can be removed by the IF filtering before the digitization of the signal. By using the polyphase filter for filtering, frequency translation and decimation the signal can be recovered at the base band. Resulting in a sampling rate, which DSP hardware can process. The polyphase filter is special type of FIR filter, and can be implemented in FPGA hardware. The critical component of this technique is the analog band pass filter at the IF frequency. This band pass filter must reduce components outside the 2.5 MHz aliasing range to an insignificant level. This filter must typically have 80dB of rejection 1.25 MHz away from the IF center frequency. The structure of the 4:1 decimation lowpass polyphase filter of figure 3 [4].

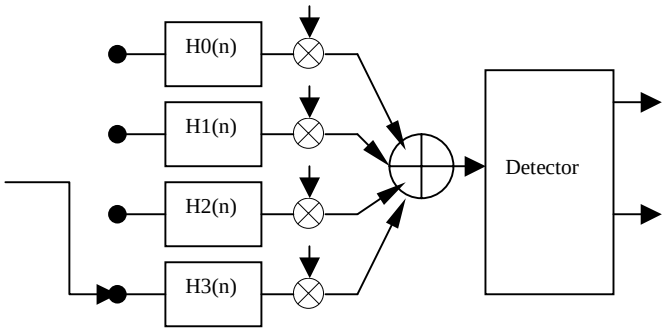

Figure 3. Polyphase filter implementation

There are several advantages of this design. First, since the signal is digitized at a lower frequency than the IF, the ADC can be a readily available dual channel 18bit audio over sampling unit with a low cost and good S/N ratio. Secondly, the Direct Digital Synthesis (DDS), sine and cosine generator of the second IF are not needed since we move all the multiplication into the polyphase filter. [4]. Thirdly, all the distortions caused by the respective analog components in the second IF are eliminated. The requirement of the IF filter are firmly stringent, but readily achievable. Finally, the design can be implement in current FPGA hardware since the computational load is reduced.

There are some disadvantages of this design. The DSP hardware requires fixed-point arithmetic, which can produce quantisation noise. The quantisation noise can be reduced if more bits are used for the digitized signal. An adequate number of bits (say 16) is achievable with current technology.

If an 18bit ADC is used, then 16 linear bits are guaranteed. A 16-bit ADC can satisfy the noise requirement. When more bits are used in the digitization, the processing complexity due to the computational load, especially the required multiplications will increase quickly. Fortunately, the available DSP hardware capabilities are also increasing quickly, doubling in speed every eighteen-month. For example, the current Xilinx Virtex II FPGA contains up to 10 million gates and several embedded 18-bit multipliers. Thus, current DSP hardware technology can now handle the load for the receiver.

IV. RF SAMPLING

The RF sampling technique is shown in figure 4.

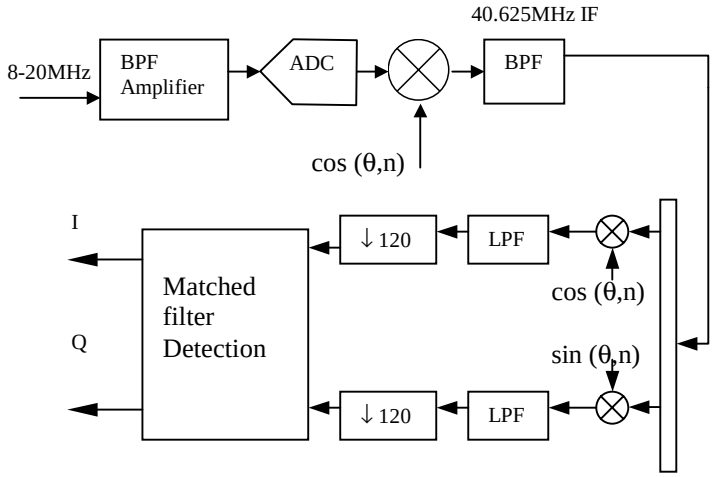

Figure 4. Block diagram of the RF sampling method

In this method, the ADC has been moved so that it directly samples the RF. The signal is sampled after the initial BPF and pre-amplifier. The sample frequency is determined by the maximum frequency required and the Nyquist sampling rate. Our maximum required frequency is 20MHz so the sampling rate must be at least 40MHz assuming a perfect band pass filter at the input. A real band pass filter will not require sufficient alternation until at least one octave and probably two octaves above the

maximum receivable frequency. A choice of 60MHz as the frequency where the stop band alternation of 80dB is to be achieved should provide an appropriate trade off between complexity of required analogue input filter and the speed of the digital FPGA implementation. Since the maximum frequency of the local digitized signal is 60MHz, the minimum sampling frequency should be 120MHz. The structure of the receiver could be similar to the analog version except everything is processed in the digital domain and the signal was down converted to a suitable rate after translation to the base band. The signal is translated to IF at 40.625 MHz and then down converted to the base band. Since the base band signal does not require high sampling rate, the signal can be decimated to a suitable rate for the detection and post processing. Alternate implementations that use time variant techniques (as discussed in section III) are also possible.

This design has advantage of using the digital domain to process all the data [8]. Hence the receiver can be compact, and there will be no tuning required after construction. There will be less error introduced by the minimal analog components in the design. However, since the sample rate is high, the computational load requires are extremely heavy and it is impractical for the current FPGA hardware to process at that sample rate. ADCs working at such a high sample rate with 16-bit resolution are also rare, and very expensive compared to the lower sample rate.

In the future, when digital technology provides resources that can practically process data at such high sampling rate, this design would provide an excellent solution for the digital receiver.

V. SIMULATION RESULTS

All the designs were simulated using the SPW package. The analog parts were simulated by using floating-point component while the digital parts were simulated by using fixed-point components with 16-bit twos-complement format.

For this analysis a DSB modulated signal centered at 8MHz, and with 100KHz bandwidth was injected into the system. Figure 5 shows the spectrum of the original signal. Figure 6 shows the spectrum of the modulated signal, which is injected into the receiver. The output of each model has been plotted.

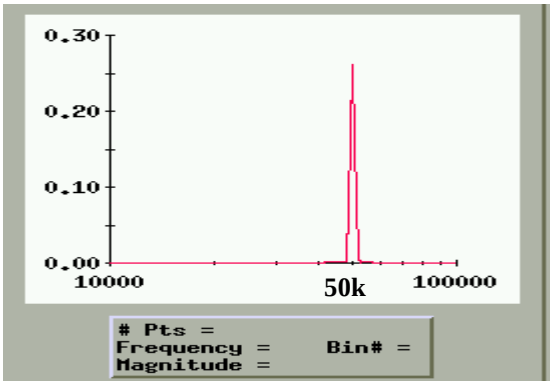

Figure 5 The spectrum of the original signal (50 KHz).

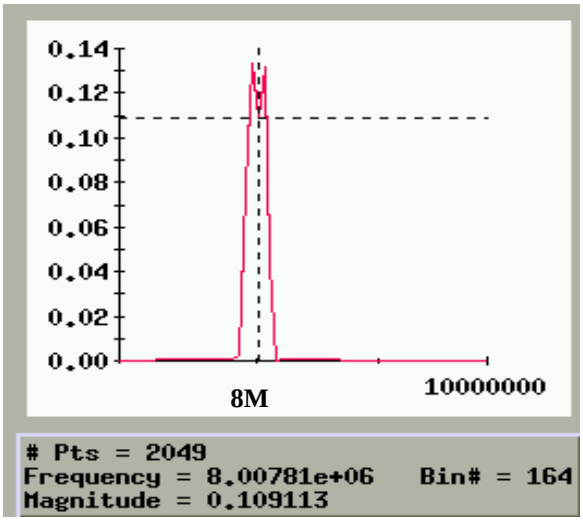

Figure 6 The spectrum of the modulated signal 8MHz, 100KHz bandwidth

Figure 7 and figure 9 show the output spectrum the two methods: direct conversion and IF under sampling respectively. As can be seen from the figures, the IF under sampling method can retrieve similar results.

Figure 8 shows the spectrum of the aliased signal. When the signal is sampled at 2.5MHz rate, the aliased carrier will be 0.625MHz. Using the polyphase filter for frequency translation, the base band signal at 50KHz can be recovered.

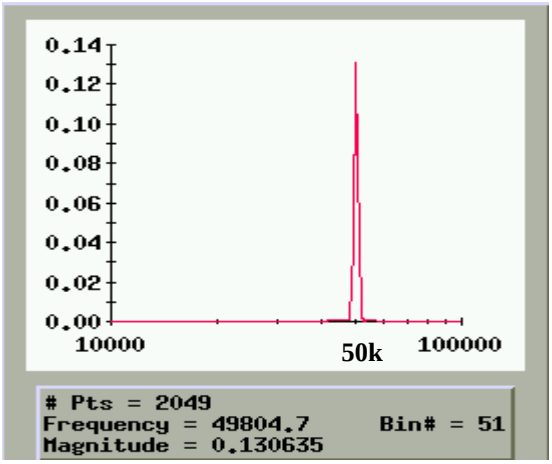

Figure 7 The output spectrum of the direct conversion method

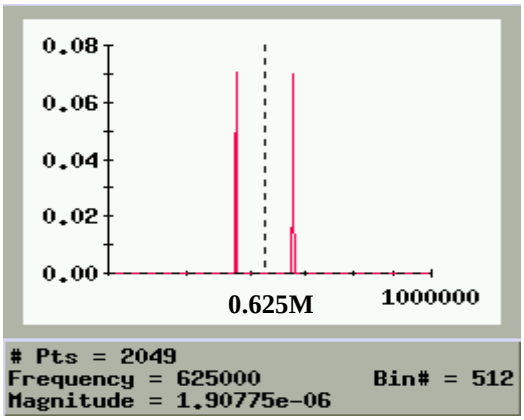

Figure 8 The spectrum of the signal after digitized at 2.5MHz. The alias frequency is 0.625MHz

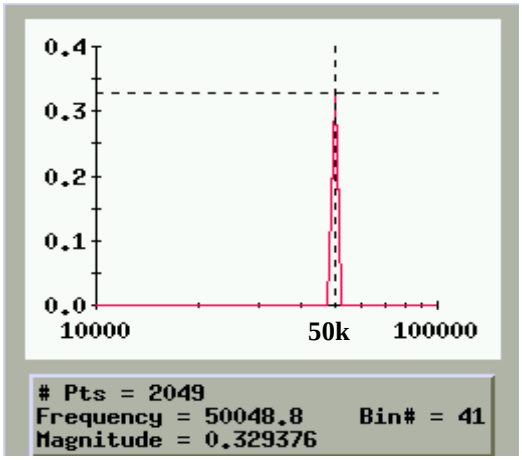

Figure 9 The output spectrum of the IF under sampling method

Since the RF sampling method is similar to the direct conversion method except that all steps are done in the digital domain, the simulation results are similar to the direct conversion method. The difference is that this method requires more computational load.

VI. CONCLUSION

Several methods for the digital implementation of the TIGER radar receiver have been discussed, including their structure, advantages and disadvantages. With current technology, the TIGER receiver can be implemented using the IF under sampling method. This method has been chosen since it provides good results with less computation. It is the best compromise between available technology and performance. The receiver will be built using FPGA technology with 16-bit two-complement data format. However, with the rapid increase in ADC and digital technology, the RF sampling method can be considered for a future design.

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